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Suppression of Current Collapse of High-Voltage AlGaN/GaN HFETs on Si Substrates by Utilizing a Graded Field-Plate Structure

Tadayoshi DEGUCHI††, Hideshi TOMITA†, Atsushi KAMADA†, Nonmembers, Manabu ARAI†, Nonmembers, Manabu ARAI†, Nonmembers, Kimiyoshi YAMASAKI†, Members, and Takashi EGAWA††, Nonmembers

SUMMARY Current collapse of AlGaN/GaN heterostructure field-effect transistors (HFETs) formed on qualified epitaxial layers on Si substrates was successfully suppressed using graded field-plate (FP) structures. To improve the reproducibility of the FP structure manufacturing process, a simple process for linearly graded SiO₂ profile formation was developed. An HFET with a graded FP structure exhibited a significant decrease in an on-resistance increase ratio of 1.16 even after application of a drain bias of 600 V.

key words: AlGaN/GaN HFETs, current collapse, field plate, on-resistance

1. Introduction

In highly efficient switch-mode power supply systems, it is essential to use high-voltage power-switching devices with low on-resistance (Ron) and high switching speed. An AlGaN/GaN hetero-structure field-effect transistor (HFET) has been studied as a promising candidate for next-generation power devices due to its high carrier mobility in two-dimensional electron gas (2DEG) and high breakdown voltage with a large critical electron field.

One of the most important aspects of developing AlGaN/GaN HFETs is suppressing current collapse, which degrades Ron during high-voltage operation. Current collapse is strongly dependent on the channel-electron acceleration due to the electric field concentration [1] and also on the quality of the epitaxial layers [2].

It is well known that Γ-shaped field-plate (FP) structures effectively suppress current collapse [3], [4]. The effects of these conventional FP structures are, however, insufficient because an electric field still concentrates at the gate and FP electrode edges. Therefore, a linearly graded FP structure is appropriate for HFETs because it disperses the electric field concentration and minimizes peak electric field strength [5]. However, there have been few reports of HFETs with these structures because of difficulties in the manufacturing process [6]. On the other hand, a decrease in yellow luminescence intensity strongly relates to current collapse [2].

We developed a simple and reproducible linearly graded FP manufacturing process and applied it to the fabrication of AlGaN/GaN Schottky barrier diodes (SBDs) and HFETs on Si substrates to investigate the effectiveness of a linearly graded FP structure on breakdown voltage and current collapse.

2. High-Voltage AlGaN/GaN SBDs

2.1 Device Fabrication

To investigate the effects of graded FP structures on breakdown voltage, AlGaN/GaN SBDs with a thick epitaxial layer utilizing anode FP and cathode FP structures were fabricated.

AlGaN/GaN hetero-structures were grown on an n-type 4-inch Si (111) substrate by metal-organic chemical vapor deposition (MOCVD). The epilayer structure consisted of, from top to bottom, a 25-nm-thick undoped Al₀.₂₆Ga₀.₇₄N layer, 1.0-μm-thick GaN layer, and 4.2-μm thick buffer layer. Detailed conditions are described elsewhere [7]. The total thickness of the epitaxial layer was 5.2 μm. The sheet resistance, the 2DEG density, and the mobility of the wafer from Hall effect measurement were 823 Ω/sq, 6.3 × 10¹²/cm², and 1200 cm²/Vs, respectively.

A 3.0-μm-thick SiO₂ layer and a 100-nm-thick phosphosilicate-glass (PSG) layer were deposited by plasma-enhanced chemical-vapor deposition (PECVD). We used Trimethyl phosphate (TMP) for doping phosphorus in PSG. After photoresist patterning, the PSG/SiO₂ films were dipped in a buffered hydrofluoric acid (BHF) solution and then etched. A linearly graded SiO₂ profile for fabricating graded FPs can be formed by exploiting the difference between the etching rates of PSG and SiO₂. The gradient angle can be controlled by increasing the etching rate ratio as phosphorus density increases.

To form cathode ohmic contacts and graded FP electrodes, Ti/Al (30/200 nm) were then deposited by electron beam evaporation and defined using a wet etching technique. Then, the samples were subjected to rapid thermal annealing (RTA) at 500°C 10 min in a N₂ ambient. After photoresist patterning and PSG/SiO₂ wet etching with the method mentioned above, the Schottky contact metals, consisting of Ni/Mo/Al (20/80/100 nm), were used to form anode Schottky contacts and graded FP electrodes. Finally, contact pads were formed by 1-μm-thick Al electrode deposition and defined by wet etching.
Figure 1 shows a cross-sectional schematic of a fabricated AlGaN/GaN SBD. The diameter of the circular Schottky contact was 90 µm, and the distance between the Schottky and ohmic contacts was 60 µm. The FP lengths of the anode and cathode contacts were both 10 µm.

2.2 Reverse Voltage Characteristics

Figure 2 shows the cumulative probability of breakdown voltage of fabricated AlGaN/GaN SBDs. The breakdown voltage characteristics were measured in fluorinert™ to prevent surface breakdown. We found that the SBDs exhibited extremely high breakdown voltages of more than 2000 V, 2500 V maximum, by utilizing a graded FP structure.

3. Suppression of Current Collapse in AlGaN/GaN HFETs

3.1 Device Fabrication

AlGaN/GaN hetero-structures were grown on an n-type 4-inch Si (111) substrate by MOCVD. The epitaxial structure consisted of, from top to bottom, a 25-nm-thick undoped Al0.28Ga0.72N layer, 1.0-µm-thick GaN layer, and 2.6-µm-thick buffer layer, as shown in Fig. 3(a). The total thickness of the epitaxial layer was 3.6 µm. The sheet resistance, the 2DEG density, and the mobility of the wafer from Hall effect measurement were 706 Ω/sq, 6.1 × 10¹²/cm², and 1450 cm²/Vs, respectively.

The source and drain ohmic contacts were formed using a lift-off technique. After photoresist patterning, the samples were dipped in a HCl: H₂O (1:1) solution to remove native oxide on the AlGaN surface. Ohmic contact metals, consisting of Ti/Al/Ti/Au (10/200/50/300 nm), were de-
posited in sequence by electron beam evaporation. The samples were then subjected to rapid thermal annealing (RTA) at 850°C for 30 sec in a N₂ ambient. After forming the ohmic contacts, device isolation was conducted by B⁺ ion implantation. Next, Ni/Au (20/530 nm) were used to form gate Schottky contacts and graded FP electrodes. Finally, a 5-µm-thick polyimide film was coated and cured at 420°C in a N₂ ambient to act as a protection layer preventing surface breakdown.

Figures 3(a), (b) and (c) show a schematic cross-sectional view, SEM image of a graded gate FP structure, and a photomicrograph of a fabricated AlGaN/GaN HFET, respectively. HFETs with circular gates 120 µm in diameter were fabricated on an epitaxial wafer. The gate length (Lg) was 2 µm, the gate-drain offset length (Lgd) was 10 µm, and the field plate length (Lfp) was 7 µm.

To investigate the effects of a graded FP structure and an epitaxial wafer on current collapse, we also used a commercially available epitaxial wafer in fabricating Al₀.₂₅Ga₀.₇₅N/GaN HFETs on conductive Si substrates with or without graded FP structures. The epilayer structure consisted of, from top to bottom, a 30-nm-thick undoped Al₀.₂₅Ga₀.₇₅N layer, 1.5-µm-thick GaN layer, and 2.3-µm-thick buffer layer. The total thickness of the epitaxial layer was 3.8 µm. The sheet resistance, the 2DEG density, and the mobility of the wafer from Hall effect measurement were 496 Ω/sq, 8.9 × 10¹²/cm², and 1414 cm²/Vs, respectively.

The Lg, Lgd, and Lfp were 10 µm, 10 µm, and 7 or 0 µm (with or without FP), respectively.

### 3.2 DC I-V Characteristics

Figures 4(a) and (b) show Iₜₐ₉−V₉ₜ and off-state characteristics of a fabricated AlGaN/GaN HFET with a graded FP using our epitaxial wafer. The Iₜₐ₉−V₉ₜ characteristics were measured using an Agilent B1500A semiconductor device analyzer, and the off-state characteristics were measured using a Tektronix 371A curve tracer.

### 3.3 Current Collapse

The R₉ₜₐ₉ increase ratio was also evaluated by comparing R₉ₜₐ₉ before and after high-voltage drain stress. Figure 5 shows the bias conditions used for measuring the R₉ₜₐ₉ increase ratio. The evaluation steps were as follows. (1) For drain current Iₜₐ₉ at a drain bias V₉ₜ of 0.5 V, a gate bias (V₉) of 0 V was measured \( \frac{0.5 (V)}{Iₜₐ₉ (A)} = R₉ₜₐ₉(before) \). (2) V₉ₜ above 100 V was applied for 10 s to a fabricated HFET while the HFET was in an off state (V₉ = −6 V). (3) The change in Iₜₐ₉ was measured at a V₉ₜ of 0.5 V and again at a V₉ of 0 V \( R₉ₜₐ₉(after) \).

Figures 6(a) and (b) show the R₉ₜₐ₉ increase ratio, defined as \( \frac{R₉ₜₐ₉(after)}{R₉ₜₐ₉(before)} \), of fabricated AlGaN/GaN HFETs using a commercially available epitaxial wafer and our epitaxial wafer. The HFET with and without FP structures formed on a commercially available epitaxial wafer, of which the R₉ₜₐ₉ increase ratios were, respectively, 1.56 and 3.39 under an applied drain voltage of 600 V. With the fabricated HFET with a graded FP using our epitaxial wafer, the R₉ₜₐ₉ increase ratio remained low (i.e., 1.16) even under
an applied drain voltage of 600 V.

To investigate the effects of GaN wafer quality on current collapse, we measured photoluminescence (PL) by using an ultraviolet He-Cd laser (325 nm). Figure 7 shows the PL spectrum of a (a) commercially available wafer and (b) our epitaxial wafer. An intense emission around 365 nm relates to the band-edge luminescence of GaN. A broad band emission around 550 nm is yellow luminescence. This yellow luminescence relates to deep-level electron traps, which cause current collapse. We used a yellow-to-band-edge luminescence intensity ratio ($I_{YL}/I_{BE}$) as an index of wafer quality because it correlates strongly with current collapse [2]. The $I_{YL}/I_{BE}$ of our epitaxial wafer was 0.75, whereas that for the commercially available epitaxial wafer was 1.20. This result indicates that the GaN epitaxial layer, which shows a low yellow luminescence intensity, suppressed current collapse and had the same tendency as reported in the above report [2].

These results indicate that using a graded gate FP structure and a qualified epitaxial wafer are key for suppressing current collapse in AlGaN/GaN HFETs.

4. Conclusion

We developed a linearly graded SiO$_2$ profile formation process with good reproducibility and fabricated AlGaN/GaN SBDs and HFETs on Si substrate by using graded FP structures. The SBDs exhibited a high breakdown voltage of 2500 V. The HFETs exhibited significant decrease in the $R_{on}$ increase ratio by 16% even after an applied drain voltage of 600 V. AlGaN/GaN electron devices with graded FP structures using qualified epitaxial wafers are promising for high-voltage power electronics application.

References


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